# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

| Attorney Docket No. | P98,2198 |
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| *First Named Inventor or Application Identifier* | |
| Kenji Ohsawa et al. | |
| *Express Mail Label No:* | |

ADDRESS TO: **Assistant Commissioner for Patents**
**Box Patent Application**
**Washington, DC 20231**

## APPLICATION ELEMENTS

*See MPEP chapter 600 concerning utility patent application contents.*

1. ☒ Specification — Total Pages 32
2. ☒ Drawing(s) (35USC 113) — Total Pages 7
3. ☒ Declaration and Power of Attorney — Total Pages 2
   a. ☐ Newly executed(original or copy)
   b. ☐ Copy from prior application (37CFR 1.63(d))
   *(for continuation/divisional with Box 14 completed)*
   ***[Note Box 4 Below]***
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting Inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
4. ☐ Incorporation By Reference (usable if Box 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

## ACCOMPANYING APPLICATION PARTS

5. ☐ Assignment Papers (cover sheet & documentation)
6. ☒ Letter under 37 CFR 1.41(c).
7. ☐ English Translation Document *(if applicable)*
8. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
9. ☐ Preliminary Amendment
10. ☒ Return Receipt Postcard (MPEP 503)
*(Should be specifically itemized)*
11. ☐ Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
12. ☒ Certified Copy of Priority Document(s)
Japanese P09-327938 filed 11-28-97
13. ☒ Other: unexecuted declaration

**14. If a CONTINUING APPLICATION**, *check appropriate box and supply the requisite information:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) ☐ of prior application No:____/____

CLAIMS AS FILED

| (1) FOR | | (2) NUMBER FILED | (3) NUMBER EXTRA | (4) RATE | (5) BASIC FEE $760.00 |
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| TOTAL CLAIMS | 20 | 13 | 0 | $18.00 | |
| INDEPENDENT CLAIMS | 03 | 3 | 0 | $78 00 | |
| | | ANY MULTIPLE DEPENDENT CLAIMS? ☒ YES ☐NO | | $260.00 | $260.00 |
| | | | | TOTAL FILING FEE -> | $1020 00 |

☒ The Commissioner is hereby authorized to charge any additional fees which may be required in connection with this application, or credit any overpayment to ACCOUNT NO. 08-2290. A duplicate copy of this sheet is enclosed.

☒ A check in the amount of $1020.00 to cover the filing fee is enclosed.

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November 24, 1998

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Re: Our Case No. P98,2198
Inventor: Kenji Ohsawa et al.
For: SEMICONDUCTOR DEVICE, METHOD MAKING THE SAME, AND ELECTRONIC DEVICE USING THE SAME

S I R:

Under the provisions of 37 CFR 1.41(c), I am filing the attached application 13 claims, Figure 1-7 on (7 sheets) and $1020.00 filing fee on behalf of

Kenji Ohsawa and Tomoshi Ohde

and request that the application be assigned a Serial Number and filing date pursuant to the provisions of 37 CFR 1.53(b) and 37 CFR 1.53(d).

Respectfully submitted,

Lewis T. Steadman (Reg. No. 17,074)
FOR THE FIRM

388/1077
Enclosures

# SEMICONDUCTOR DEVICE, METHOD MAKING THE SAME, AND ELECTRONIC DEVICE USING THE SAME

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to a semiconductor device, a method for making the same, and to an electronic device utilizing the semiconductor device.

### 2. Description of the Related Art

In recent years, various wire-bond-type chip size packages (CSPs) have appeared in response to multi-electrode trends of semiconductor chips. Among the different types of CSPs, FIG. 7A shows a flexible printed circuit (FPC) type CPS. The FPC type CPS comprises a base **a** composed of a polyimide resin, and wiring films **b** composed of a metal such as copper formed on the surface of the base **a**. Holes **c** for forming electrodes (herein after referred to as "electrode-forming holes **c**") are formed in the base **a**, and fine spherical electrodes **d** composed of solder are formed in the electrode-forming holes **c**. A semiconductor chip **f** placed on the base **a** is bonded to the base **a** with a silver-paste film **e**. Gold bonding wires **g** connect electrodes of the semiconductor chip **f** with the corresponding wiring films **b**. The semiconductor chip **f** and the bonding wires **g** are sealed

with a sealing resin **h**.

FIG. 7B shows a rigid substrate type CPS. The rigid substrate type CPS comprises a rigid wiring substrate **i** having holes (through-holes) **j** for forming electrodes (hereinafter referred to as electrode-forming holes), wiring films **k** formed on the rigid wiring substrate **i**, and wiring films **l**. The wiring films **l** are connected to the wiring films **k**, functions as an external electrode, and does not require solder spherical electrodes. A semiconductor chip **f** is placed on an insulating film **m** composed of a resist between the wiring films **k**, and is bonded to the insulating film **m** with a silver-paste film **e**. Gold bonding wires **g** connect electrodes of the semiconductor chip **f** with the corresponding wiring films **k**. The semiconductor chip **f** and the bonding wires **g** are sealed with a sealing resin **h**.

Although the FPC type CPS shown in FIG. 7A has an advantage of a high rate of heat dissipation, it does not allow electroplating since fine solder spherical electrodes are in the wiring films **b** which are electrically isolated from each other. Thus, it is significantly difficult to form fine solder spheres. Since it is impossible to reduce the diameter of the electrode-forming holes **c**, reduction in the array pitch between the hole-electrodes is limited. Accordingly, the appearance of the electrode-forming holes and of the spherical electrodes is inferior. Since the

wiring films **b** are formed by selective etching, production of a fine pattern is limited. Furthermore, the base **a** is flexible; hence workability is inferior and production of large devices is difficult.

Although the rigid substrate type has an advantage that no solder spherical electrode is formed, it is difficult to reduce the diameter of the electrode-forming holes to 0.35 mm or less. This is a factor limiting higher integration of semiconductor devices. Furthermore, production of a fine wiring film pattern is difficult, the appearance of the electrode-forming holes is inferior, and heat dissipation is slow. Since the electrode-forming holes are formed by drilling, production is difficult.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a CSP- or BGA-type semiconductor device that allows mounting of fine spherical electrodes.

It is another object of the present invention to provide a CSP- or BGA-type semiconductor device that achieves miniaturization of electrode-forming holes, fineness of a wiring film pattern, improved appearance, and simplified production process.

A first aspect of the present invention is a semiconductor device comprising: a plurality of wiring films

formed on a front surface of a base comprising an insulating resin and having electrode-forming holes, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes; a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base; a semiconductor element positioned on the front surface of the base with an insulating film therebetween, the back surface of the semiconductor element being bonded to the front surface of the base; and wires for bonding the electrodes of the semiconductor element to the corresponding wiring films.

Since the wiring films are formed on a front surface section of the base so as to embed them; surface steps are not formed. Since a sodium chloride is mounted onto the surface, bonding of the semiconductor device and wire bonding are readily performed, resulting in enhancing reliability of the semiconductor device. Since the electrode-forming holes are formed by exposure and development of the base, fineness and high integration permitting large-scale integration and multi-electrodes of the semiconductor device can be achieved.

A metal ring may be bonded on the front surface of the base at the exterior of the connecting sections with wires

in the wiring films. In such a preferred embodiment, the ring is used as an electrical power source, for example, a ground source, as an electrostatic shield for electrostatically shielding between the semiconductor device and the exterior, and as a dam for preventing leakage of the sealing resin to the exterior.

A second aspect of the present invention is A method for making a film circuit comprising: a step of forming wiring films on a metal film for stopping etching as an underlying layer by plating using a mask film, the mask being selectively formed on a front surface of a metal substrate; a step of forming a base comprising an insulating resin and having electrode-forming holes on the front surface of the metal substrate such that at least parts of the wiring films are partly exposed; and a step of etching at least the region of the metal substrate, in which the wiring films are formed, from the back surface until the metal film for stopping etching is exposed.

Since the electrode-forming holes can be formed by patterning of the insulating resin on the metal substrate, fining of the electrode-forming holes can be achieved. Thus, the diameter of the electrode-forming holes can be reduced to 0.22 mm or less, whereas the lower limit of the diameter is 0.25 mm for a conventional FPC type, or 0.35 mm for a rigid substrate type. Such fining of the electrode-forming

holes can increase the array density of the electrode-forming holes. The electrode-forming holes can be formed by patterning the insulating resin with a reduced working load and increased productivity compared with the formation of electrode-forming holes by drilling as in the rigid substrate type.

Preferably, the metal film for stopping etching is deposited on the surface of the metal substrate, a mask film is selectively formed on the metal film for stopping etching, and the wiring films are formed on the metal film as an underlying layer through the mask film by plating; and the metal film for stopping etching is deposited on the surface of the metal substrate; a mask film is selectively formed on the metal film for stopping etching, and the wiring films are formed on the metal film as an underlying layer through the mask film by plating; and after completing the etching step for exposing the metal film for stopping etching from the back surface at least in the region of the metal substrate in which the wiring films are formed, the metal film for stopping etching is removed.

The region, in which at least wiring films are formed, of the metal substrate is etched from the back surface so that the underlying metal film for etching stop is exposed and the metal substrate remains as a ring at the exterior. Thus, the remaining section can be used as a ring. The ring

can be used as a ground electrical source terminal and an electrostatic shield, as described above. Since the ring forms an outer shape of the semiconductor device and is formed by etching, working accuracy can be increased. Thus, the semiconductor device has high shape accuracy.

Since it is produced using a metal substrate as a mother material, deformation such as distortion will not occur during the production. Thus, working is easy. A large semiconductor device, therefore, can be readily formed.

A third aspect of the present invention is an electronic device comprising a semiconductor device comprising: a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes; a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base; a semiconductor element positioned on the a front surface of the base with an insulating film therebetween, the back surface of the semiconductor element being bonded to the front surface of the base; and wires for bonding the electrodes of the semiconductor element to the corresponding wiring films.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1I are cross-sectional views showing steps of a first embodiment of a method for making a semiconductor device of the present invention;

Figs. 2A and 2B are enlarged cross-sectional views illustrating the states after forming the bases when a separable resist film and an inseparable resist film, respectively, are used as resist films in the first embodiment;

Fig. 3A is a cross-sectional view when a solder plating film is formed on nickel films as external electrodes, and Fig. 3B is a cross-sectional view when the solder plating film is shaped by reflow;

Fig. 4A is a cross-sectional view showing a conventional array pitch of the external electrodes; Fig. 4B is a cross-sectional view showing an array pitch in accordance with the present invention; and Fig. 4C is a plan view showing that the wiring films between the external electrodes are increased in this embodiment.

Figs. 5A to 5K are cross-sectional views of steps of a second embodiment of the method for making the semiconductor device in accordance with the present invention;

Fig. 6 is a partly broken isometric view of an electronic device using a semiconductor device of the

present invention; and

Figs. 7A and 7B are cross-sectional views of a flexible printed circuit (FPC) type wire-bonding CSP and a rigid substrate type wire-bonding CSP.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A semiconductor device of the present invention comprises a plurality of wiring films formed on a front surface of a base composed of an insulating resin and having electrode-forming holes, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes; a conductive material embedded into the electrode-forming holes to form external electrodes protruding from the back surface of the base; a semiconductor element positioned on the front surface of the base with an insulating film therebetween, the back surface of the semiconductor element being bonded to the front surface of the base; wires for bonding the electrodes of the semiconductor element to the corresponding wiring films.

The semiconductor device can be produced by a method for making a semiconductor device comprising: a step of forming wiring films on a metal film for stopping etching as an underlying layer by plating using a mask film, the mask being selectively formed on a front surface of a metal

substrate; a step of forming a base composed of an insulating resin and having electrode-forming holes on the front surface of the metal substrate such that at least parts of the wiring films are partly exposed; and a step of etching at least the region of the metal substrate, in which the wiring films are formed, from the back surface until the metal film for stopping etching is exposed.

The metal substrate functions as a base material in the production of the semiconductor device including the formation of the wiring films and external electrodes by plating and as passage of a plating current, although it may later form an outer ring. It is preferable that the metal substrate comprise copper or a copper-based material having high conductivity. Since these materials have significantly high rigidity, they are not flexible even when thin, and thus have high workability. It is preferable that the thickness be approximately 150 μm when copper or a copper-based material is used.

A photosensitive separable acrylic resist can be used as a mask film during plating for forming the wiring films. In this case, the mask film is formed by patterning including exposure and development and then the wiring films are formed using the mask film. After the plating treatment, the mask film is peeled off. An epoxyacrylic photosensitive eternal resist film (having a thickness of, for example, 40

μm) may be used. Also, in this case, the mask film is formed by patterning including exposure and development and the wiring films are formed by plating using the mask film. After the plating treatment, however, the resist film is not removed, although the mask film is peeled off. Thus, the surface of the wiring film and the surface of the base are positioned completely on the same plane; in other words, the surface is planarized. Nickel electrodes will be formed without deformation in the subsequent step, since the underlying layer does not have a stepped structure. The material is not limited to the above-mentioned one. For example, materials that function as masks when a wiring film of metal such as copper is formed are usable.

As a base, for example, a laminate film of a polyamic acid-type polyimide film and a photosensitive layer provided thereon (thickness: for example, 25 μm) may be used. The laminate film is patterned by exposing and developing the photosensitive layer, and then etching the polyamic acid-type polyimide film with an etching solution such as an alkaline solution. The polyamic acid-type polyimide film is sufficiently cured by heat treatment at 280°C for approximately 30 minutes. The thickness of the resist mask film is, for example, approximately 25 μm. The entire mask film may be formed of a photosensitive resin and be patterned by exposure to form electrode-forming holes. In

the formation of the base, various modifications are possible.

It is preferable that the wiring film be formed by plating copper on a nickel underlayer. Although the wiring film is formed by plating on a metal substrate composed of, for example, copper, it is difficult to deposit by directly plating a dense copper wiring film on the copper. Furthermore, when the wiring film is exposed by etching the metal substrate, an etching stopper is necessary to protect the copper wiring film from being etched. Nickel is most suitable for the etching stopper. The thickness of the nickel film may be, for example, 2 μm. It is preferable that the thickness of the copper wiring film be, for example, 25 μm, although it depends on the specifications and performance demands of the semiconductor device.

After forming the base having electrode-forming holes, external electrodes are formed by plating, for example, nickel with a thickness of 40 to 150 μm thereon. Alternatively, they may be formed by plating nickel in a thickness of approximately 100 μm and then by plating solder in a thickness of approximately 100 μm, and by reflow-shaping the solder. Accordingly, various modifications are available for the formation of the external electrodes.

The metal substrate is etched from the back surface. Although the etching is essential for exposure of the wiring

film, it may be performed on the entire surface or may be performed selectively. In selective etching, the etching is preferably performed in a region in which the wiring film is formed so that the metal substrate is left as a peripheral ring. The peripheral ring can be used as a reinforcing element, a ground electrode and an electrostatic shielding element of the electrical power source, and a dam for blocking the flow of the sealing resin (in the case of CSP). Thus, selective etching is preferred to complete etching. Etching can be performed using an alkaline etchant (ammonia type) that can etch copper but cannot etch nickel. Thus, nickel can function as an etching stopper.

It is preferable that the external electrode be formed of nickel and the surface of the nickel plating film be plated with gold, in view of satisfactory contact formation. Preferably, an underlayer is generally provided for gold plating. In this case, the external electrode and the metal film for stopping etching are formed of nickel; hence it is not necessary to form an additional nickel underlayer for satisfactory gold plating. Of course, the present invention is applicable to the above-mentioned embodiment in which the external electrode is formed of nickel and a solder plating film, and other embodiments.

The present invention is applicable to both CPS-type and BGA-type semiconductor devices.

The semiconductor device in accordance with the present invention can be used in various electronic devices, and in particular, compact electronic devices, such as portable phones, and contributes to miniaturization and improvement in reliability of the devices.

Preferred embodiments of the present invention will be described in detail with reference to the attached drawings. Figs. 1A to 1I are cross-sectional views showing the steps of a method for making a CSP-type semiconductor device as a first embodiment of the present invention.

With reference to Fig. 1A, a metal substrate 1 composed of copper or a copper alloy with a thickness of 50 to 250 μm is prepared, and a resist film 2 or a mask film with a thickness of 30 to 60 μm is selectively formed. A typical resist is an acrylic photosensitive separable resist or an epoxyacrylic photosensitive inseparable resist. The resist is patterned by exposure and development to form a mask film 2.

With reference to Fig. 1B, a copper wiring film 4 having a nickel underlayer 3 is formed on the surface of the metal substrate 1 using the resist film 2 as a mask. The thickness of the copper wiring film 4 is in a range of approximately 15 to 30 μm, and is preferably 25 μm. The thickness of the nickel underlayer 3 is in a range of approximately 1 to 5 μm, and is preferably 2.5 μm. The

nickel underlayer 3 blocks etching of the copper wiring film 4 when the metal substrate 1 is etched from the back surface to expose wiring. Thus, the nickel underlayer 3 functions as a metal film for stopping etching. Alternatively, a metal substrate 1 with an entire nickel underlayer 3 provided thereon may be used and the entire nickel underlayer 3 may be etched to avoid short-circuiting between wiring films 4 after the etching to expose wiring. Although this configuration will be described in a second embodiment, it can also be applied to this embodiment.

When the resist film 2 is of an acrylic photosensitive separable type, it is removed. In contrast, when the resist film 2 is of an epoxyacrylic photosensitive inseparable type, it is not removed. A base 5 (thickness: for example 25 μm) composed of, for example, a polyimide resin is formed and patterned to form electrode-forming holes 8 and smaller vent holes 10 at given positions. Fig. 1C shows a state after the patterning. Vent holes 10 release gas formed in the bottom of the base 5 in order to prevent separation of the base 5 due to thermal expansion during heat treatment.

The base 5 may be composed of, for example, a laminate film of a polyamic acid-based polyimide film and a photosensitive layer provided thereon. The base 5 is patterned by exposing and developing the photosensitive layer, and then etching the polyamic acid-type polyimide

film with an etching solution such as an alkaline solution. The polyamic acid-type polyimide film is sufficiently cured by heat treatment at 280°C for 30 minutes. The entire mask film may be formed of a photosensitive resin and may be patterned by exposure to form electrode-forming holes 8.

Figs. 2A and 2B are enlarged cross-sectional views illustrating the states of the bases 5 when a separable resist film 2 and an inseparable resist film 2, respectively, are used. When the inseparable resist is used, the residual section 2a of the resist film 2 remains on the substrate 1. When the inseparable resist is used, the surface of the wiring film 4 and the surface of the base 5 can be arranged on substantially the same plane; that is, the surface is planarized. Nickel electrodes 6 will be formed without deformation in the subsequent step, since they are formed on the flat surface. In these two cases, the spaces between the adjacent wiring films 4 (the nickel films 3) are embedded by the base 5 so that the base 5 and the wiring films 5 form a flat surface.

With reference to Fig. 1D, a nickel film 6 is deposited in the electrode-forming holes 8 by electroplating to form spherical electrodes. The thickness of the plating layer is approximately 40 to 150 μm.

With reference to Fig. 1E, the metal substrate 1 is selectively etched from the back surface so that it remains

as a peripheral ring 9 at the peripheral section of each semiconductor device while the wiring film 4 is exposed on the nickel underlayer 3. An ammonia-type alkaline etchant is used for etching. The nickel underlayer 3 blocks etching of the copper wiring film 4. A gold film 7 (thickness: for example, 0.3 to 6 μm) is formed by plating on the nickel films 3 and 6. The gold film 7 is depicted in the enlarged external electrode 6 that is shown in the bottom section of Fig. 1E, although it is not depicted in the drawings after Fig. 1E, for the sake of convenience.

With reference to Fig. 1F, a heat dissipating plate 12 (thickness: for example, 100 μm) composed of copper or a 42 alloy is bonded to the front surface of the base 5 by a bonding agent 11 (thickness: for example, 50 μm). The heat dissipating plate 12 enhances heat dissipation from the semiconductor device that will be subsequently mounted.

A semiconductor element 14 is die-bonded on the heat dissipating plate 12 with, for example, a silver-paste film 13, followed by wire bonding. Fig. 1G shows a state after the wire bonding. Each wire 15 composed of, for example, gold, connects an external electrode of the semiconductor element 14 and the wiring film 4 covered with the nickel underlayer 3 through the gold film 7 (not depicted in Fig. 1G). The nickel underlayer 3 and the gold film 7 on the wiring film 4 enhance wire bonding strength, since the

surface gold film 7 has a high affinity for the gold wire 15 and the underlying nickel underlayer 3 blocks ultrasonic waves which are applied for bonding.

With reference to Fig. 1H, the semiconductor element 14 and its peripheral section are sealed with a sealing resin 16. The peripheral ring 9 functions as a dam blocking the flow of the resin towards the outside.

With reference to Fig. 1I, the nickel external electrode 6 is shaped substantially spherically by, for example, reflow. Alternatively, a solder plating film 17 may be formed on the nickel film 6 as the external electrode 6 with a thickness of, for example, 50 to 100 μm as shown in Fig. 3A, and then may be shaped by reflow as shown in Fig. 3B. A semiconductor device is thereby produced.

In the semiconductor device shown in Fig. 1I, a plurality of wiring films 4 are formed on a surface section of a base 5 comprising an insulating resin, so that the surfaces of the wiring films 4 and the surface of the base 5 are positioned on the same plane and at least parts of the wiring films 4 overlap the electrode-forming holes 8 of the base 5. Each of the electrode-forming holes 8 is embedded with a nickel film 6 as a conductive material to form a protruding external electrode. A heat dissipating plate 12 is bonded to the surface of the base 5 with a cushion bond 11. The semiconductor element 14 is bonded to the heat

dissipating plate 12 with a silver-paste film 13. Each electrode of the semiconductor element 14 is bonded to the corresponding wiring film 4 with a wire 15. Furthermore, the wiring film 4 and the wire 15 are sealed with a resin 15.

In this semiconductor device, the wiring film 4 is formed on a surface section of the base 5 so as to be embedded; hence the front surface of the base 5 is planarized. Since the semiconductor element 14 is mounted on the flat surface, bonding and wiring of the semiconductor device can be readily performed, resulting in enhanced reliability of the semiconductor device. Since the semiconductor element 14 is provided on the surface without a stepped structure, die bonding and wire bonding characteristics of the semiconductor element 14 are improved and wiring films with a fine pattern can readily formed. Since the electrode-forming holes 8 are formed by exposure and development of the base 5, fining and high integration of the electrode-forming holes 8 can be achieved. Thus, high integration and multi-electrodes of the semiconductor device can also be achieved. Since the base 5 has vent holes 10, separation of the base 5 due to a popcorn phenomenon is prevented.

Since the peripheral metal ring 9 is provided at the exterior of the wire bonding sections of the wiring films 4 on the surface of the base 5, the peripheral ring 9 can be

used as a ground electrode of an electrical power source, and as a electrostatic shield that electrostatically shields the semiconductor element 14 from the exterior. Also, it can be used as a dam that blocks the flow of the sealing resin to the exterior when resin sealing is performed, resulting in a decreased defect rate of the resin sealing.

In the method for making the semiconductor device shown in Figs. 1A to 1I, wiring films 4 are formed by plating using a resist film as a mask which is selectively formed on a front surface of the metal substrate 1, wherein nickel films 3 for etching stop are formed as an underlayer. A base 5 composed of an insulating resin and having electrode-forming holes 8 and vent holes 10 is formed on the front surface of the metal substrate 1. The region of the metal substrate 1 in which at least the wiring films 4 are formed is etched from the back surface until the nickel film 3 for etching stop is exposed. Furthermore, a semiconductor element 14 is mounted onto the etched side and sealed with a resin.

According to such a method, the wiring films 4 are formed on the metal substrate 1 by plating using the resist film 2 as a mask, electrode-forming holes 8 are formed in a base 8, and then external electrodes 6 are formed by plating. Thus, the wiring films 4 and the external electrodes 6 are easily formed by electroplating, because the metal substrate

1 is electrically connected to all of the wiring films 4 so that a potential required for electroplating is applied to all of the wiring films 4 through the metal substrate 1. Since electroplating can form a plating film having higher quality than that of electroless plating, satisfactory wiring films 4 and external electrodes 6 are readily formed. Thus, fine, high-density arrangement of the wiring films 4 and the external electrodes 6 can be achieved. With fineness of the wiring films, the number of the wiring films that are provided between the external electrodes can be increased; hence the number of the external electrode arrays and the number of the external electrodes can be increased.

Fig. 4A is a cross-sectional view showing a conventional array pitch of the external electrodes. Fig. 4B is a cross-sectional view showing an array pitch in accordance with the present invention. Fig. 4C is a plan view showing that the wiring films between the external electrodes are increased in this embodiment. In a typical conventional FPC-type semiconductor device in which fine patterning is difficult, the width of the wiring film 4 is 500 μm for the portion for forming the external electrodes 6, or 50 μm between the external electrodes 6, and the distance between the wiring films 4 is 50 μm. Thus, when the pitch of the external electrode array is decreased, the number of wiring films 4 between the external electrodes 6 cannot be

increased. In contrast, fine patterning can be performed in this embodiment; hence the number of the wiring films 4a between the external electrodes 6 can be increased as shown in Fig. 4C even when the pitch of the external electrode array is decreased, permitting a multiple spherical electrode array. This significantly contributes to multi-electrodes and high integration of semiconductor devices.

Since the electrode-forming holes 8 can be formed by patterning the base 5 on the metal substrate 1, finesse of the electrode-forming holes 8 is achieved. The size of the electrode-forming holes 8 can be reduced to 0.22 mm or less in a rigid substrate type, whereas its lower limit is 0.5 mm for a conventional FPC type or 0.35 mm for a conventional rigid substrate type. Finesse of the electrode-forming holes 8 results in a higher array density of the electrode-forming holes 8. The electrode-forming holes 8 are formed by patterning the insulating resin, hence working is not troublesome and productivity is high compared with a method requiring drilling of the holes.

The region for forming the wiring films 4 of the metal substrate 1 is etched from the back surface until the nickel metal underlayer 3 for etching stop is exposed, so that the metal substrate 1 remains as a ring 9 at its exterior. The ring 9 can be used as a terminal of the ground electrical power source, and for electrostatic shielding, as described

above. The ring 9 is formed in the peripheral region by etching, with high working accuracy. Thus, the semiconductor device has a peripheral form which is highly accurate.

In the production process of the semiconductor device, the metal substrate 1 is used as a base material, thus, deformation such as distortion does not occur in the production process. Thus, handling and working are facilitated. The peripheral ring 9 may be removed to miniaturize the semiconductor device in some cases. Since the resin 16 has reinforcement effects after resin sealing, the peripheral ring 9 also having reinforcement effects is not always essential and may be omitted in some cases. In such a case, the peripheral ring 9 may be removed to miniaturize the semiconductor device.

Figs. 5A to 5K are cross-sectional views of the steps of a method for making a BGA-type semiconductor device in accordance with the present invention, as a second embodiment.

With reference to Fig. 5A, a laminate film of a thin copper or copper alloy film 1 with a thickness of, for example, 150 μm and a nickel film 3 provided thereon for etching stop with a thickness of, for example, 2 μm is prepared as a metal substrate.

With reference to Fig. 5B, copper wiring films 4 with a

thickness of, for example, 25 μm are selectively formed as follows. Resist films are selectively formed on the surface of the nickel film 3 to form a mask, and copper films 4 are plated on the nickel film 3 using the mask. The process is substantially the same as that in the first embodiment. Thus, the wiring films 4 are selectively formed by the same method as in the first embodiment. In the first embodiment, however, the metal substrate is composed of copper or a copper alloy not having a surface nickel film, hence a nickel film 3 for etching stop is formed by plating using a resist film as a mask, and then the copper wiring films 4 are formed by plating. In the second embodiment, the nickel film 3 has already been formed on the metal substrate, and the formation of the nickel film 3 by plating is not necessary.

With reference to Fig. 5C, bases 5 composed of polyimide are selectively formed as in the first embodiment to form electrode-forming holes 8 and vent holes 10 which are considerably smaller than the electrode-forming holes 8.

With reference to Fig. 5D, nickel films 6 are deposited in the electrode-forming holes 8 by plating so as to protrude from the electrode-forming holes 8. Solder films 16 with a thickness of, for example, approximately 100 μm are formed on the nickel films 6 with a thickness of 40 to 150 μm.

With reference to Fig. 5E, the copper portion on the metal substrate 1 is selectively etched so that the surface of the nickel film 3 is exposed and the metal substrate 1 is left as a peripheral ring 9 at the peripheral section. In the etching, the nickel film 3 blocks etching of the copper wiring films 4, that is, functions as a metal film for stopping etching.

With reference to Fig. 5F, the nickel film 3 for etching stop is removed by etching, because the nickel film 3 formed on the entire surface of the substrate 1 will cause short-circuiting if it is allowed to remain. In contrast, in the first embodiment, the nickel films 3 and the wiring films 4 are formed by the same pattern, hence etching between the wiring films is not necessary, and this step is not provided.

A dam 18 is formed on the surface after removing the nickel film 3 by, for example, a screen printing process, so that it blocks the flow of the resin during the resin sealing process. The dam 18 is formed as a ring at the peripheral section of the resin-sealing region of the semiconductor device that will be bonded later.

With reference to Fig. 5G, a semiconductor element 14 is bonded with a cushion bond 11. Next, with reference to Fig. 5H, wire bonding is performed using wires 15. With reference to Fig. 5I, the semiconductor element 14 is sealed

with a resin. With reference to Fig. 5J, a reinforcing member 19 is bonded with a bonding agent 20.

With reference to Fig. 5K, the reinforcing member 19 is bonded to the peripheral ring 9 with, for example, a silver paste 21. The silver paste 21 is applied and is subjected to reflow between the reinforcing member 19 and the peripheral ring 9. A semiconductor device in the second embodiment of the present invention is thereby formed.

The semiconductor device and the method for making the semiconductor device in accordance with the second embodiment also have similar advantages to those of the first embodiment. In the second embodiment, a possible modification is a metal substrate 1 not having a surface nickel film 3 as in the first embodiment. The peripheral ring 9 may be removed later to achieve miniaturization of the semiconductor device, because the reinforcing member 19 sufficiently develops the reinforcing and electrostatic functions in place of the peripheral ring 9.

The semiconductor device can be used in various electronic devices, and particularly meets the high demands of miniaturization in, for example, portable phones. Fig. 6 shows an electronic device A or a portable phone, in which a semiconductor device C in accordance with the present invention is mounted as an internal circuit of the electronic device onto a mother board B.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes;

a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base;

a semiconductor element positioned on said front surface of the base with an insulating film therebetween, the back surface of the semiconductor element being bonded to said front surface of the base; and

wires for bonding the electrodes of the semiconductor element to the corresponding wiring films.

2. A semiconductor device according to claim 1, wherein said semiconductor element and said wires are sealed with a resin.

3. A semiconductor device according to claim 1, wherein a metal ring is bonded on the front surface of the

base at the exterior of the connecting sections with wires in the wiring films.

4. A semiconductor device according to claim 1, wherein said semiconductor element and said wires are covered with a reinforcement having a downward indented face.

5. A semiconductor device according to any one of claims 1 to 4, wherein the base has vent holes.

6. A method for making a film circuit comprising:

a step of forming wiring films on a metal film for stopping etching as an underlying layer by plating using a mask film, the mask being selectively formed on a front surface of a metal substrate;

a step of forming a base comprising an insulating resin and having electrode-forming holes on the front surface of the metal substrate such that at least parts of the wiring films are partly exposed; and

a step of etching at least the region of the metal substrate, in which the wiring films are formed, from the back surface until the metal film for stopping etching is exposed.

7. A method for making a film circuit according to

claim 6, wherein said metal film for stopping etching is formed by using the mask after said mask is formed and before the wiring films are formed.

8. A method for making a film circuit according to claim 6, wherein

the metal film for stopping etching is deposited on the surface of the metal substrate;

a mask film is selectively formed on the metal film for stopping etching, and the wiring films are formed on the metal film as an underlying layer through the mask film by plating; and

after completing the etching step for exposing the metal film for stopping etching from the back surface at least in the region of the metal substrate in which the wiring films are formed, the metal film for stopping etching is removed.

9. A method for making a semiconductor device using a film circuit according to claim 6, comprising a step of forming external electrodes in the electrode-forming holes and a step of electrically connecting the wiring films and the electrodes of the semiconductor device.

10. A method for making a semiconductor device using a

film circuit according to claim 7, comprising a step of forming external electrodes in the electrode-forming holes and a step of electrically connecting the wiring films and the electrodes of the semiconductor device.

11. An electronic device comprising a semiconductor device comprising: a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes; a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base; a semiconductor element positioned on said a front surface of the base with an insulating film therebetween, the back surface of the semiconductor element being bonded to said front surface of the base; and wires for bonding the electrodes of the semiconductor element to the corresponding wiring films.

12. An electronic device according to claim 11, wherein said semiconductor element and said wires are sealed with a resin.

13. An electronic device according to claim 11, wherein said semiconductor element and said wires are covered with a reinforcement having a downward indented face.

ABSTRACT OF THE DISCLOSURE

In a semiconductor device, a plurality of wiring films are formed on a front surface of a base comprising an insulating resin and having electrode-forming holes, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes; a conductive material is embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base; a semiconductor element is positioned on the front surface of the base with an insulating film therebetween, the back surface of the semiconductor element being bonded to said front surface of the base; wires bond the electrodes of the semiconductor element to the corresponding wiring films; and a resin seals the wiring films and the wires.

FIG. 1A

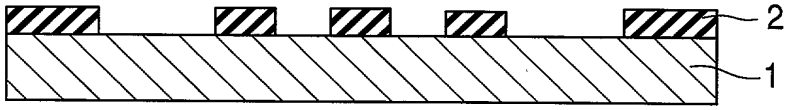



FIG. 1B

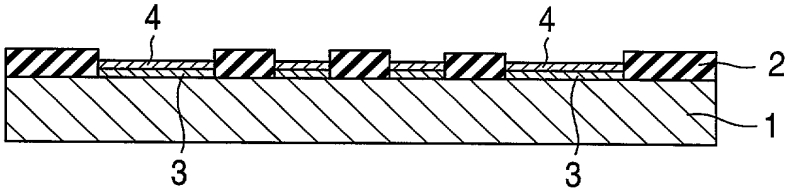



FIG. 1C

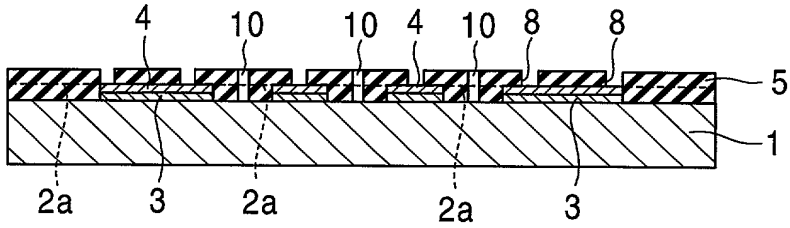



FIG. 1D

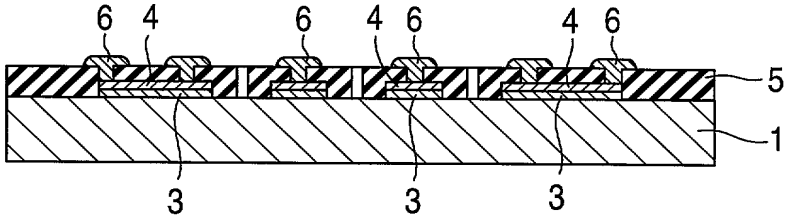



FIG. 1E

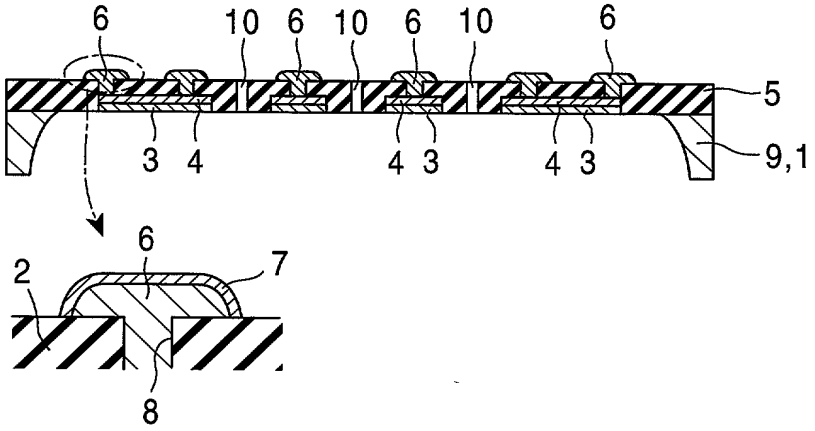


FIG. 1F

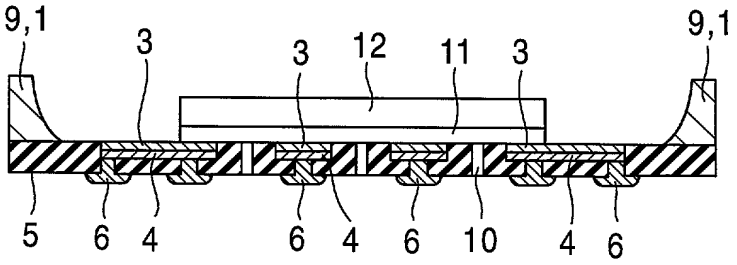



FIG. 1G

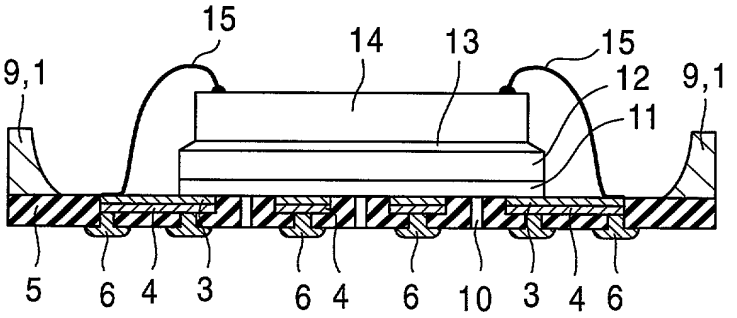



FIG. 1H

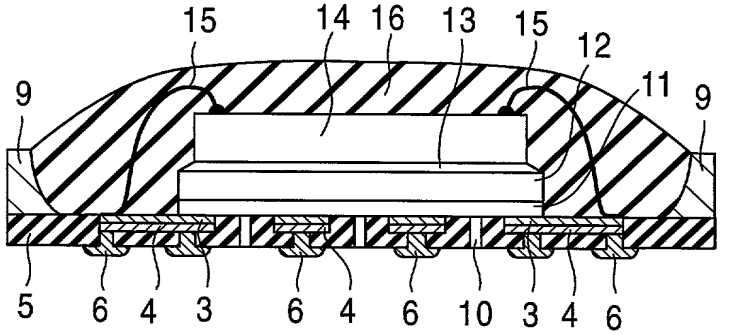



FIG. 1I

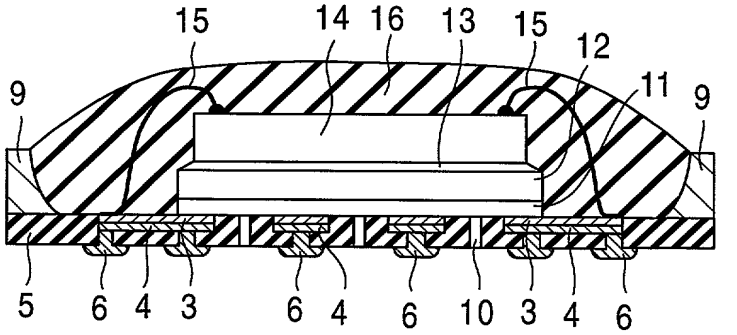


FIG. 2A

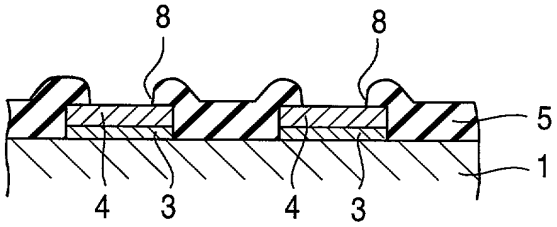



FIG. 2B

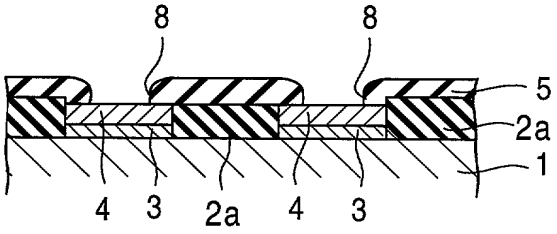



FIG. 3A

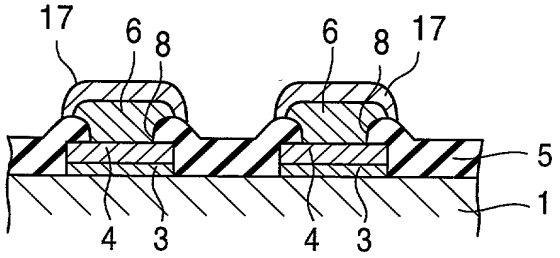



FIG. 3B

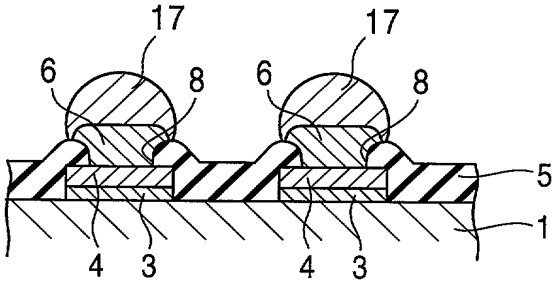


FIG. 4A

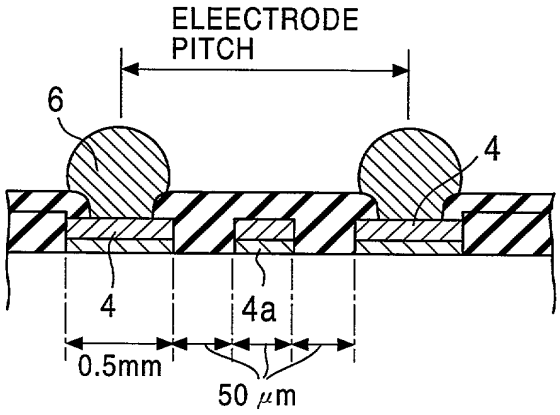



FIG. 4B

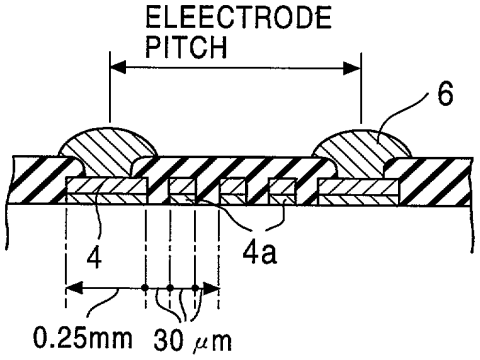



FIG. 4C

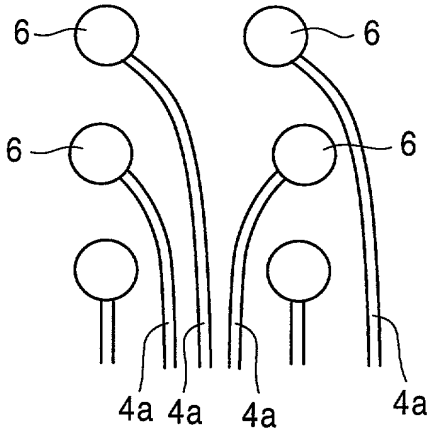


FIG. 5A

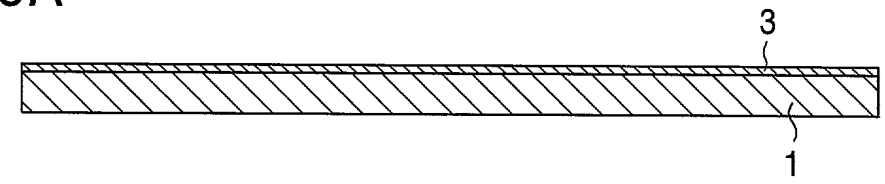



FIG. 5B

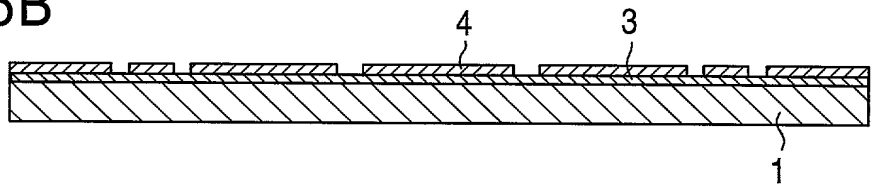



FIG. 5C

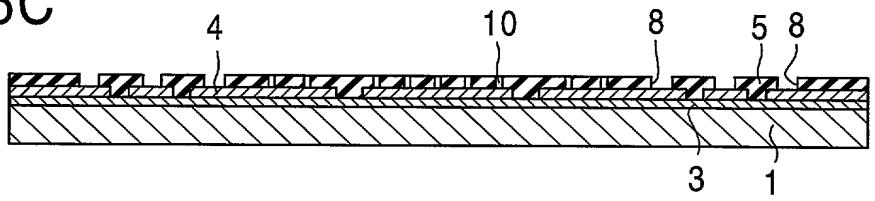



FIG. 5D

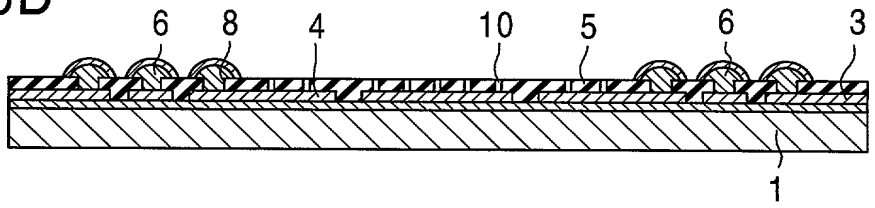



FIG. 5E

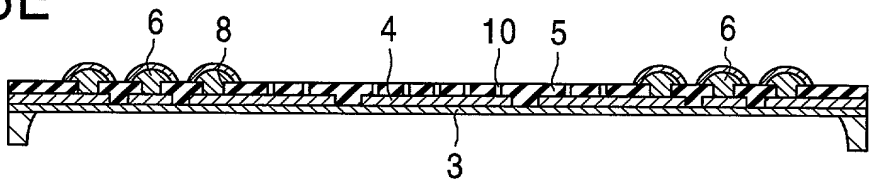



FIG. 5F

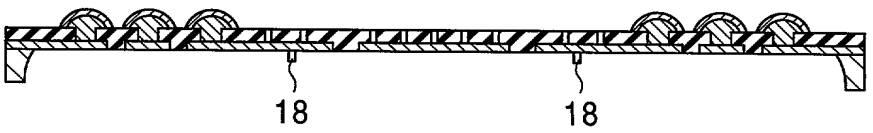
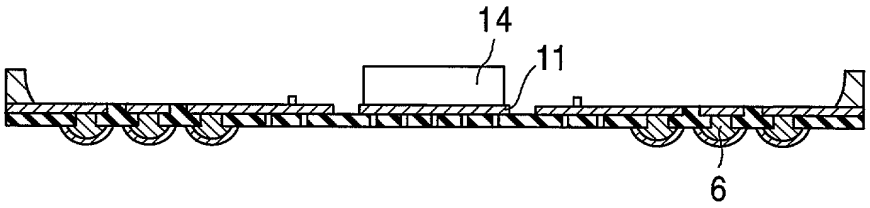


FIG. 5G




HIG. 5H

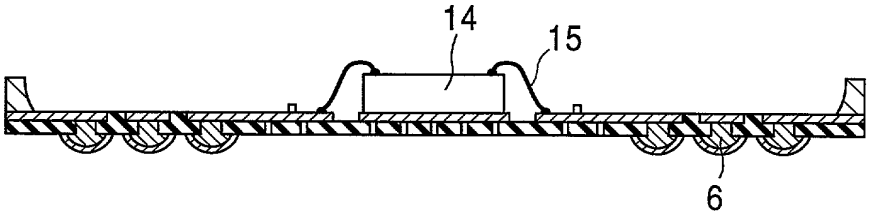



FIG. 5I

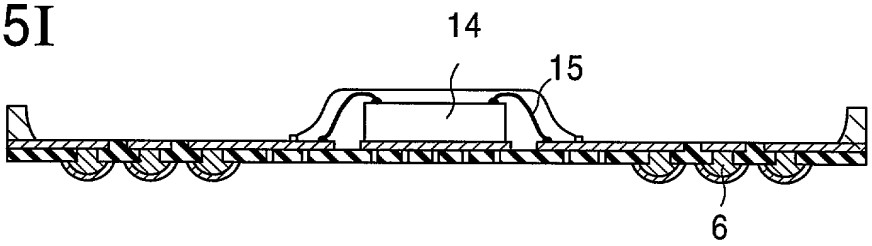



FIG. 5J

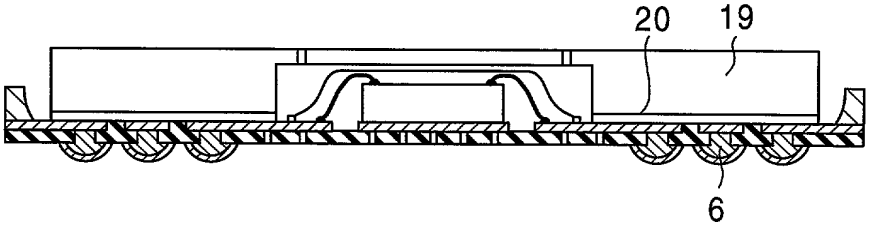



FIG. 5K

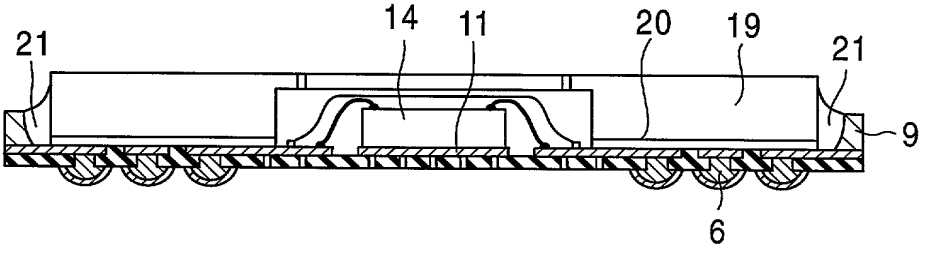


FIG. 6

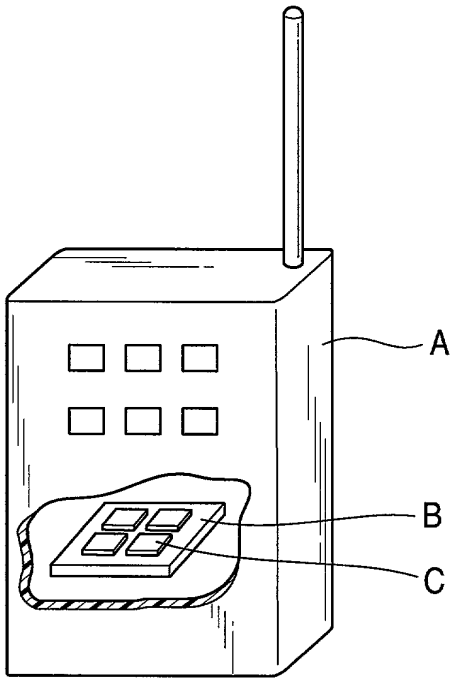



FIG. 7A

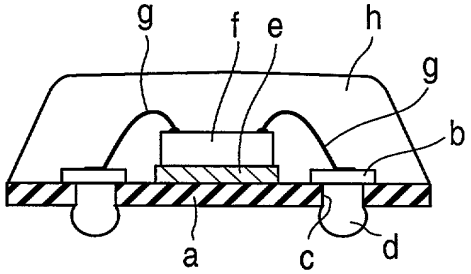
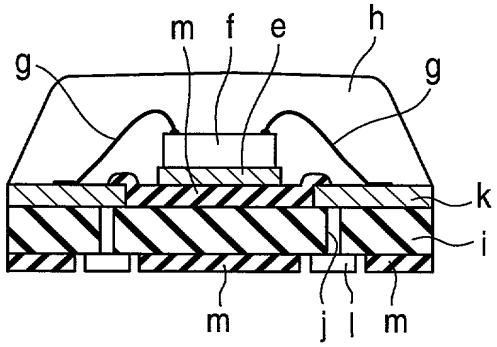



FIG. 7B



# DECLARATION AND POWER OF ATTORNEY

*As a below named inventor, I hereby declare that:*

*My residence, post office address and citizenship are as stated below next to my name,*

*I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:*

***SEMICONDUCTOR DEVICE, METHOD MAKING THE SAME, AND ELECTRONIC DEVICE USING THE SAME***

*Case No.* ***P98,2198*** *, the specification of which*

| | | |
|---|---|---|
| | X | *is attached hereto.* |
| *(check* | ___ | *was filed on* _____, *as* |
| *one)* | | *Application Serial No.* _____ |
| | | *and was amended on* _____. |
| | | *(if applicable)* |

*I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.*

*I acknowledge the duty to disclose to the United States Patent Office all information which is known to me to be material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, 1.56(a).*[1]

*I do not know and do not believe this invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and I believe that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as identified below:*

*I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below*

*Prior Foreign Application(s)*

| *Number* | *Country* | *Date* |
|---|---|---|
| *P09-327938* | *Japan* | *November 28, 1997* |

---

[1] *(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and*

*(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or*

*(2) It refutes, or is inconsistent with, a position the applicant takes in:*

*(i) Opposing an argument of unpatentability relied on by the Office, or*

*(ii) Asserting an argument of patentability.*

*A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.*

*and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the above listed application on which priority is claimed:*

*Prior Foreign Application(s)*

| *Number* | *Country* | *Date* |
|---|---|---|

*If no priority is claimed, I have identified all foreign patent applications filed prior to this application:*

*Prior Foreign Application(s)*

| *Number* | *Country* | *Date* |
|---|---|---|

*And I hereby appoint Messrs. John D. Simpson (Registration No. 19,842), Lewis T. Steadman (17,074), Dennis A. Gross (24,410), Robert M. Barrett, (30,142), Steven H. Noll (28,982), Kevin W. Guynn (29,927), Robert M. Ward (26,517), Brett A. Valiquet (27,841), Edward A. Lehman (22,312), David R. Metzger (32,919), Todd S. Parkhurst (26,494), James D. Hobart (24,149), Melvin A. Robinson (31,870), John R. Garrett (27,888), Paula J. Kelly (37,624), John W. Cornell (30,619), Robert J. Depke (37,607), Joseph P. Reagan (35,332), Michael R. Hull (35,902), Michael S. Leonard (37,557), William E. Vaughan (39,056) and Marvin Moody (16,549) all members of the firm of Hill & Simpson, A Professional Corporation*

*Telephone: 312/876-0200 Ext. 3388*

*my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and direct that all correspondence be forwarded to:*

*Hill & Simpson*
*A Professional Corporation*
*85th Floor Sears Tower, Chicago, Illinois 60606*

*I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.*

*Full name of sole or first inventor* KENJI OHSAWA

*Inventor's signature* _____ *Date* _____
*Residence* Kanagawa, Japan
*Citizenship* Japan
*Post Office Address* c/o Sony Corporation, 7-35, Kitashinagawa 6-Chome,
Shinagawa-Ku, Tokyo, Japan

*Full name of second joint inventor, (if any)* TOMOSHI OHDE

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